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Agrawal et al.

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(45) Date of Patent: **Jan. 30, 2001**

(54) **FPGA INTEGRATED CIRCUIT HAVING
EMBEDDED SRAM MEMORY BLOCKS AND
INTERCONNECT CHANNEL FOR
BROADCASTING ADDRESS AND CONTROL
SIGNALS**

5,744,980 4/1998 McGowan et al. 326/40
6,046,603 * 4/2000 New 326/41
6,049,223 * 4/2000 Lytle et al. 326/41

FOREIGN PATENT DOCUMENTS

WO 98/10517 12/1998 (WO) H03K/19/177

* cited by examiner

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patent shall be extended for 0 days.

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(52) U.S. Cl. **326/41; 326/39**

(58) Field of Search **326/37-41**

(56) **References Cited**

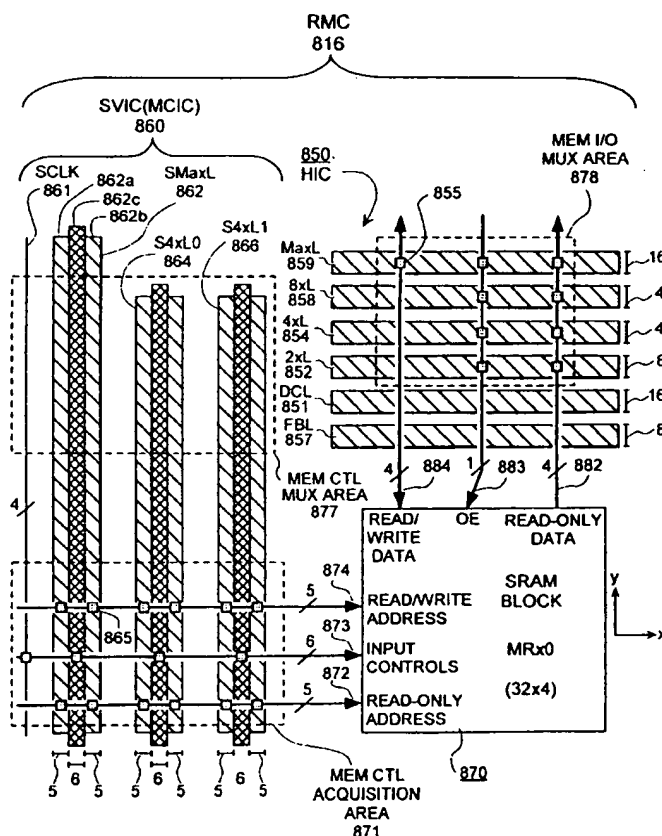
U.S. PATENT DOCUMENTS

5,550,782 8/1996 Cliff et al. 365/230.03

(57) ABSTRACT

A field-programmable gate array device (FPGA) having plural rows and columns of logic function units (VGB's) further includes a plurality of embedded memory blocks, where each memory block is embedded in a corresponding row of logic function units. Each embedded memory block has an address port for capturing received address signals and a controls port for capturing supplied control signals. Interconnect resources are provided including a Memory Controls-conveying Interconnect Channel (MCIC) for conveying shared address and control signals to plural ones of the memory blocks on a broadcast or narrowcast basis.

17 Claims, 27 Drawing Sheets



	L #	Hits	Search Text	DBs
1	L1	82086	(port set group) near10 (pin pad)	USPAT; US-PGPUB
2	L2	17157	((i adj2 o) input\$4 output\$4 connector connection) near20 1	USPAT; US-PGPUB
3	L3	76108	(port pin pad) near20 ((select\$5 reconfigur\$4 configur\$4 switch\$4 multiplex\$3) near20 (interfac\$3 connect\$3 interconnect\$3 coupl\$3))	USPAT; US-PGPUB
4	L4	1435	2 near99 3	USPAT; US-PGPUB
5	L5	5063	3 near20 ((process\$3 function\$3 operation\$3 core internal\$2 inside chip) near10 (resource element unit module device peripher\$2))	USPAT; US-PGPUB
6	L6	112	2 near99 5	USPAT; US-PGPUB
7	L7	29555	(port set group) near10 (pin pad)	EPO; JPO; DERWENT; IBM_TDB
8	L8	3811	((i adj2 o) input\$4 output\$4 connector connection) near20 7	EPO; JPO; DERWENT; IBM_TDB
9	L9	19578	(port pin pad) near20 ((select\$5 reconfigur\$4 configur\$4 switch\$4 multiplex\$3) near20 (interfac\$3 connect\$3 interconnect\$3 coupl\$3))	EPO; JPO; DERWENT; IBM_TDB
10	L11	1024	9 near20 ((process\$3 function\$3 operation\$3 core internal\$2 inside chip) near10 (resource element unit module device peripher\$2))	EPO; JPO; DERWENT; IBM_TDB
11	L12	14	8 near99 11	EPO; JPO; DERWENT; IBM_TDB
12	L10	172	8 near99 9	EPO; JPO; DERWENT; IBM_TDB

	Document ID	U	Title	Current OR
1	JP 20031 43031 A	<input type="checkbox"/>	INITIAL ADJUSTMENT METHOD FOR CARD-TYPE WIRELESS TRANSMISSION DEVICE	
2	JP 20030 99187 A	<input checked="" type="checkbox"/>	TOUCH PAD INPUT DEVICE AND OPERATING FUNCTION SWITCHING METHOD	
3	JP 20012 51328 A	<input checked="" type="checkbox"/>	MULTIPLEX PORT ETHERNET (R) UNIT, AND METHOD AND SYSTEM FOR MINIMIZING EXTERNAL PIN	
4	JP 20010 84754 A	<input checked="" type="checkbox"/>	SEMICONDUCTOR INTEGRATED CIRCUIT AND MEMORY MODULE PROVIDED THEREWITH	
5	WO 83034 88 A1	<input checked="" type="checkbox"/>	AUTOMATIC CIRCUIT IDENTIFIER	
6	US 20020 02660 6 A	<input checked="" type="checkbox"/>	Integrated circuit with embedded memory and on-chip testing circuit, has controller coupled to multiplexer to select subset of data lines among data lines of internal bus coupled to embedded memory device	
7	US 20020 00606 6 A	<input checked="" type="checkbox"/>	Flash memory device for testing wafer chips, has switch circuits which are connected between memory array and data input-output pins, such that data input-output pins correspond to number of switch groups	
8	JP 11327 456 A	<input checked="" type="checkbox"/>	IC chip terminal connecting structure in flat surface liquid crystal display device - is configured by electrically connecting input-output terminal group of IC chip with one of connection pad group	
9	US 58217 76 A	<input checked="" type="checkbox"/>	Mixed signal integrated circuit device with FPGA structure - has programmable interconnecting elements in field programmable gate array, which are arbitrarily connected between segments of conductors and input-output nodes of analog and digital modules	
10	EP 69680 1 A	<input checked="" type="checkbox"/>	Synchronous semiconductor memory device for DRAM microprocessor - uses selected bits of internal address to access memory section and select groups of internal data lines at different frequency	
11	TW 27018 9 A	<input checked="" type="checkbox"/>	Connector assembly for peripheral device - has pin arrangement configured for use by peripheral device, and determination system for communication mode of peripheral device	
12	EP 57396 5 A	<input checked="" type="checkbox"/>	Semiconductor device with multiple function selection bonding optional circuit according to power source or ground connection - has two transistors connected in parallel between bond pad and voltage terminal, of different drive capability, with larger drive transistor turned ON only for set time after device power-up, and has circuit to output pad potential signal	
13	EP 51784 6 B	<input checked="" type="checkbox"/>	Programmable logic device with programmable inverters at I=0 - including two sets of programmable lines crossing one another and connectable by programming links at each section	
14	SU 10769 01 A	<input type="checkbox"/>	Number sorter with selectively alterable sorting group width - has code input unit taken across logic modules to pin board connected to logic function generators taken to AND-gates	

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1	JP 20031 43031 A	<input type="checkbox"/>	INITIAL ADJUSTMENT METHOD FOR CARD-TYPE WIRELESS TRANSMISSION DEVICE	
2	JP 20030 99187 A	<input checked="" type="checkbox"/>	TOUCH PAD INPUT DEVICE AND OPERATING FUNCTION SWITCHING METHOD	
3	JP 20030 99105 A	<input checked="" type="checkbox"/>	METHOD AND SYSTEM FOR CONFIGURING INPUT/OUTPUT POINT	
4	JP 20021 10913 A	<input checked="" type="checkbox"/>	CIRCUIT DESIGN PATTERN FOR TESTING SEMICONDUCTOR CIRCUIT	
5	JP 20020 50199 A	<input checked="" type="checkbox"/>	NON-VOLATILE SEMICONDUCTOR MEMORY HAVING TESTING FUNCTION	
6	JP 20012 51328 A	<input checked="" type="checkbox"/>	MULTIPLEX PORT ETHERNET (R) UNIT, AND METHOD AND SYSTEM FOR MINIMIZING EXTERNAL PIN	
7	JP 20010 84754 A	<input checked="" type="checkbox"/>	SEMICONDUCTOR INTEGRATED CIRCUIT AND MEMORY MODULE PROVIDED THEREWITH	
8	JP 20010 59340 A	<input checked="" type="checkbox"/>	JOINT FOR SQUARE BATTER	
9	JP 20002 93277 A	<input checked="" type="checkbox"/>	INTERFACE FUNCTION SELECTING METHOD	
10	JP 20002 70047 A	<input checked="" type="checkbox"/>	TELEPHONE SET	
11	JP 20002 15655 A	<input checked="" type="checkbox"/>	RECORDING DEVICE AND JIG FOR CONNECTING INTERFACE	
12	JP 20000 22076 A	<input checked="" type="checkbox"/>	MACRO MODULE CONTROL DEVICE AND METHOD	
13	JP 11185 180 A	<input checked="" type="checkbox"/>	FIRE SENSOR, TESTER AND TESTING METHOD FOR SENSOR TYPE	
14	JP 11110 874 A	<input checked="" type="checkbox"/>	TRAY FOR DIGITAL DISK	
15	JP 11074 780 A	<input checked="" type="checkbox"/>	PROGRAMMABLE LOGIC UNIT	
16	JP 11039 245 A	<input checked="" type="checkbox"/>	SEMICONDUCTOR DEVICE CONTROLLER AND SEMICONDUCTOR DEVICE CONTROL METHOD	
17	JP 10115 655 A	<input checked="" type="checkbox"/>	SYSTEM FOR DETECTING FAULTY CABLE CONNECTION, ITS USAGE METHOD, AND CONNECTING CABLE USED FOR THE SYSTEM	
18	JP 10063 379 A	<input checked="" type="checkbox"/>	INTELLIGENT DRIVE CIRCUIT FOR EXTERNAL DATA DRIVE	
19	JP 09288 724 A	<input checked="" type="checkbox"/>	OBSERVED IMAGE DATA PROCESSOR	

	Docum ent ID	U	Title	Current OR
20	JP 09181 183 A	<input checked="" type="checkbox"/>	SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE	
21	JP 09107 702 A	<input checked="" type="checkbox"/>	TAIL WHEEL AND MOUNT FOR LEVEE FORMER IN ROTARY RIDGING MACHINE	
22	JP 08064 648 A	<input checked="" type="checkbox"/>	SEMICONDUCTOR WAFER	
23	JP 07142 996 A	<input checked="" type="checkbox"/>	FIELD PROGRAMMABLE GATE ARRAY DEVICE	
24	JP 07055 884 A	<input checked="" type="checkbox"/>	TIME SHARING CONNECTING CIRCUIT FOR TESTING INTEGRATED CIRCUIT	
25	JP 06233 455 A	<input checked="" type="checkbox"/>	POWER SUPPLY SWITCHING DEVICE	
26	JP 06195 965 A	<input checked="" type="checkbox"/>	SEMICONDUCTOR STORAGE DEVICE	
27	JP 05282 394 A	<input checked="" type="checkbox"/>	SEMICONDUCTOR INTEGRATED CIRCUIT DESIGN BACK-UP DEVICE	
28	JP 05215 815 A	<input checked="" type="checkbox"/>	IC TESTING DEVICE	
29	JP 05174 562 A	<input checked="" type="checkbox"/>	COMPACT DISC REPRODUCER	
30	JP 05151 310 A	<input checked="" type="checkbox"/>	LOGIC CIRCUIT OPTIMIZATION PROCESSING METHOD	
31	JP 05013 662 A	<input checked="" type="checkbox"/>	MULTICHIP MODULE	
32	JP 04367 368 A	<input checked="" type="checkbox"/>	SOLDERING DEVICE	
33	JP 04111 294 A	<input checked="" type="checkbox"/>	SEMICONDUCTOR MEMORY	
34	JP 04096 596 A	<input checked="" type="checkbox"/>	PROCESSING METHOD OF PIN FOR LINE CONNECTION OF MAIN DISTRIBUTING BOARD OF EXCHANGE BY ROBOT	
35	JP 04057 497 A	<input checked="" type="checkbox"/>	SECURITY WIRELESS TRANSMITTER	
36	JP 04043 801 A	<input checked="" type="checkbox"/>	AIR MOTOR WITH CRANK SYSTEM	
37	JP 03242 946 A	<input checked="" type="checkbox"/>	CIRCUIT BOARD FOR HYBRID FUNCTION CIRCUIT	
38	JP 03083 410 A	<input checked="" type="checkbox"/>	SWITCH SIGNAL DISCRIMINATION CIRCUIT	
39	JP 03061 706 A	<input checked="" type="checkbox"/>	MULTIMODE AIR RELAY	
40	JP 02126 335 A	<input checked="" type="checkbox"/>	EMULATION DEVICE	
41	JP 02084 851 A	<input checked="" type="checkbox"/>	TELEPHONE SET	
42	JP 01212 952 A	<input checked="" type="checkbox"/>	TELEPHONE SYSTEM	

	Docum ent ID	U	Title	Current OR
43	JP 01208 950 A	<input checked="" type="checkbox"/>	TELEPHONE SET BRANCH CIRCUIT	
44	JP 01208 949 A	<input checked="" type="checkbox"/>	TELEPHONE SET BRANCH CIRCUIT	
45	JP 01175 251 A	<input checked="" type="checkbox"/>	SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE	
46	JP 01082 177 A	<input checked="" type="checkbox"/>	DECIDING METHOD FOR CONNECTING SECTION OF POWER SUPPLY WIRING	
47	JP 62271 001 A	<input checked="" type="checkbox"/>	CONTROLLER FOR AUTOMATIC FARM MACHINE	
48	JP 61200 741 A	<input checked="" type="checkbox"/>	LINE CONNECTOR	
49	JP 61054 077 A	<input checked="" type="checkbox"/>	METHOD FOR CONTROLLING PAD ACTION	
50	JP 61051 689 A	<input checked="" type="checkbox"/>	MAGNETIC BUBBLE CASSETTE MEMORY	
51	JP 57210 724 A	<input checked="" type="checkbox"/>	SWITCHING CIRCUIT FOR STATE SETTING	
52	JP 57103 187 A	<input checked="" type="checkbox"/>	SEMICONDUCTOR STORAGE ELEMENT	
53	EP 12940 97 A2	<input checked="" type="checkbox"/>	Input/output buffer supporting multiple I/O standards	
54	DE 10128 922 A1	<input checked="" type="checkbox"/>	Hands free set adaptor cable for cars, has selection of power supply adaptors and connectors with pin housings plugged into coupling block or black box unit	
55	EP 91394 3 A2	<input checked="" type="checkbox"/>	Integrated circuit assembly having output pads with programmable characteristics and method of operation	
56	WO 98116 96 A1	<input checked="" type="checkbox"/>	A METHOD AND SYSTEM FOR REDUCING THE PIN COUNT REQUIRED FOR THE INTERCONNECTIONS OF CONTROLLER DEVICES AND PHYSICAL DEVICES IN A NETWORK	
57	EP 69680 1 A2	<input checked="" type="checkbox"/>	Synchronous semiconductor memory device with low power consumption	
58	EP 43812 7 A2	<input checked="" type="checkbox"/>	Semiconductor wafer.	
59	EP 17975 0 A2	<input checked="" type="checkbox"/>	Modular distribution frame.	
60	WO 85011 67 A1	<input checked="" type="checkbox"/>	CONNECTION UNIT FOR INTERCONNECTING INTERCORRESPONDING ELECTRIC APPARATUS	
61	EP 93188 A1	<input checked="" type="checkbox"/>	Device for data registration, in particular for discrete registration of fluid levels.	
62	WO 83034 88 A1	<input checked="" type="checkbox"/>	AUTOMATIC CIRCUIT IDENTIFIER	
63	US 66542 14 B	<input checked="" type="checkbox"/>	Die for analog circuits, has switched capacitor circuit with groups of voltage reference input ports and electrostatic discharge resistors coupled to pad, where each resistor is coupled to unique group of ports	
64	US 20030 19752 1 A	<input checked="" type="checkbox"/>	Removable interface adapter for automatic electronic device test system, has interconnected sets of spring loaded pins configured for connection to test head and device under test board, respectively	

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65	US 65981 09 B	<input checked="" type="checkbox"/>	Printed circuit board for mini peripheral component interconnect card, has switches to selectively couple card connector pins to signal lines of non-standard PCI component and pins of component interface	
66	KR 20030 37479 A	<input checked="" type="checkbox"/>	Apparatus for detecting temporary opening of battery using scr	
67	US 65049 67 B	<input checked="" type="checkbox"/>	MEMS switching device has optical fiber output ports with passive alignment mechanism, so that they are precisely aligned to movable mirrors using respective alignment mechanisms	
68	US 65325 57 B	<input checked="" type="checkbox"/>	Integrated circuit has control circuit that selects internal signals of functional unit block for transmission to output pad, in response to reception of data indicating that signals are to be tested	
69	US 20030 01894 4 A	<input checked="" type="checkbox"/>	Semiconductor integrated circuit includes signal generation circuit whose input ports are connected to specific input pins of test access port cores, for generating selection signals in response to input signals	
70	US 20030 01457 3 A	<input checked="" type="checkbox"/>	Control circuit for configuring connector pins of input/output module, has multiple ports to output control signal for controlling pin configuration	
71	DE 10128 922 A	<input checked="" type="checkbox"/>	Hands free set adaptor cable for cars, has selection of power supply adaptors and connectors with pin housings plugged into coupling block or black box unit	
72	CN 13818 85 A	<input checked="" type="checkbox"/>	I/O port with high voltage tolerance and electrostatic discharge protection circuit	
73	TW 50458 0 A	<input checked="" type="checkbox"/>	Apparatus for examining switch matrix - with the capability of decreasing test time and the production cost	
74	US 20020 11390 8 A	<input checked="" type="checkbox"/>	Remote control handset for television set, operates multiple items of electrical apparatus by actuating function switching pin of SCART connector	
75	US 20020 10125 8 A	<input checked="" type="checkbox"/>	Programmable logic circuit for field programmable gate array, includes set of routing lines which is coupled to programmable switches to form programmable access lines functioning as input/output pins for logic blocks	
76	JP 20021 61857 A	<input checked="" type="checkbox"/>	Scroll compressor for refrigerator, has switching element provided to inverter and electrically connected with stator coil of motor by pressfitting terminal pins into grooves of connector	
77	US 63967 66 B	<input checked="" type="checkbox"/>	Semiconductor memory e.g. SDRAM has banks with memory cells and input/output units for sensing and amplifying state of data output from memory cells, and multiplexers connected between banks and pad groups	
78	US 20020 02660 6 A	<input checked="" type="checkbox"/>	Integrated circuit with embedded memory and on-chip testing circuit, has controller coupled to multiplexer to select subset of data lines among data lines of internal bus coupled to embedded memory device	
79	US 20020 01991 9 A	<input checked="" type="checkbox"/>	Control chipset for computer motherboard, has dual-function data pins connected to multiplexer and demultiplexer respectively having input terminals and output terminals of two-types	
80	US 20020 00606 6 A	<input checked="" type="checkbox"/>	Flash memory device for testing wafer chips, has switch circuits which are connected between memory array and data input-output pins, such that data input-output pins correspond to number of switch groups	
81	TW 45768 8 A	<input checked="" type="checkbox"/>	Input/output port with high voltage tolerance - and the related circuit for ESD protection	
82	US 62929 07 B	<input checked="" type="checkbox"/>	Interface apparatus for state machine and output pins of digital system, includes multiplexer to select state-machine bit group and second multiplexer to output this bit group or normal system signals, in response to control circuit	

	Docum ent ID	U	Title	Current OR
83	JP 20012 51328 A	<input checked="" type="checkbox"/>	Multiple port ethernet device has multiplexer that outputs common port status signal through bus connected to external pin of ethernet device and port effectiveness signal indicating output of status signal	
84	KR 20010 48535 A	<input checked="" type="checkbox"/>	Automatic switching apparatus and method between office line call and internet call using hook flash or special button	
85	US 61924 20 B	<input checked="" type="checkbox"/>	Integrated circuit controller for Universal Serial Bus (USB), has memory with N input terminals for storing VID and PID codes connected to an interface with N diodes, switches and transistors with connected VIDS pin to set up value of N	
86	US 61924 31 B	<input checked="" type="checkbox"/>	Computer system integrated circuit with pin-out configuration selection, using multiplexer coupled to configurable electrical connector IO ports by configured parallel bus signal lines	
87	CN 12741 16 A	<input checked="" type="checkbox"/>	Module and method for testing communication port	
88	JP 20002 77694 A	<input checked="" type="checkbox"/>	Pin array switching circuit for semiconductor device, has fail safe circuit which turns off data output pin when connection of setting pin is abnormal	
89	DE 19933 257 A	<input checked="" type="checkbox"/>	Semiconducting IC, especially microcontroller with flexible external equipment interface, has I/O pins configurable to output 3 sets of signals selected from read, write, address strobe signal group	
90	JP 20000 31388 A	<input checked="" type="checkbox"/>	Input-output interface for integrated circuit device, has selection unit which chooses part of bonding pad included in pad group confirmed, based on potential applied to input	
91	JP 11327 456 A	<input checked="" type="checkbox"/>	IC chip terminal connecting structure in flat surface liquid crystal display device - is configured by electrically connecting input-output terminal group of IC chip with one of connection pad group	
92	JP 11288 583 A	<input checked="" type="checkbox"/>	Model switching system for a floppy disc drive - has control circuit which has pin assigned for every input-output pin of interface, in which specification pin can be set by switching mode setting pin of control circuit	
93	US 59283 41 A	<input checked="" type="checkbox"/>	Control circuit in dynamic printer-port switcher for selectively connecting peripheral devices to personal computer	
94	JP 11104 039 A	<input checked="" type="checkbox"/>	Opening-closing mechanism drive unit of lid of western style toilet fixture - has two connectors which are selectively connected to pin to open and close toilet seat based on rotation direction of following board operated by lever	
95	US 58754 70 A	<input checked="" type="checkbox"/>	Multi-port multi-bank dynamic random access memory (DRAM) chip	
96	DE 29823 122 U	<input checked="" type="checkbox"/>	Plug-in component group with active-passive switching	
97	US 58675 75 A	<input checked="" type="checkbox"/>	Telephone interface card - for add-on sound boards connected to a personal computer	
98	US 58226 10 A	<input checked="" type="checkbox"/>	Distributed computer system - includes controller that regulates connection of functional circuits with input-output pins through selected connectors	
99	US 58217 76 A	<input checked="" type="checkbox"/>	Mixed signal integrated circuit device with FPGA structure - has programmable interconnecting elements in field programmable gate array, which are arbitrarily connected between segments of conductors and input-output nodes of analog and digital modules	
100	US 63891 22 B	<input checked="" type="checkbox"/>	Switching system for controlling different loads by manual or remote control switch - recognises acceptable subscriber who inputs password, and confirms turn-ON/OFF state of loads connected to switching unit via voice signal to control turn-ON/OFF to given load by key-pad input to telephone set	

	Docum ent ID	U	Title	Current OR
101	US 57621 54 A	☒	Electrical driving system for wheelchair - is installed on wheelchair by coupling together upper and lower connectors of coupling assembly about each of tipping levers of wheelchair	
102	US 57457 95 A	☒	SCSI connector and Y cable apparatus for computer system - includes switching logic which is coupled to connector and SCSI controller which receives second SCSI signals and selectively provides SCSI signal to pins of connector if dual channel cable is detected	
103	JP 10090 372 A	☒	Testing apparatus for integrated circuit - has several voltage variable devices which are provided in switch group for connecting input or output pin with high or low voltage sources respectively	
104	JP 10041 159 A	☒	Tap switching apparatus for transformers - has connecting rods which couple parallelly set of connection pieces which couple tap pins of different tap pin groups of transformer	
105	US 57015 15 A	☒	Analog wireless cellular telephone interface for PC card module for portable computer mobile communications - has switches in note-book computer which re-assign pins on 68-pin connector to audio lines in note-book, and switches in PC module which re-assign same pins to audio lines in PC module to allow voice applications on note-book computer	
106	US 57001 94 A	☒	Programmable joy-pad for playing personal computer games - has data input pin coupled to computer, clock pin coupled to computer, set pin coupled to parallel/serial conversion circuit via direction mode switch	
107	KR 97071 218 A	☒	Serial port switching circuit for computer system	
108	US 56747 81 A	☒	Multilayer interconnects in semiconductor processing - by forming titanium/titanium nitride stack interconnect structures which can be used as local interconnects and landing pads on the same level	
109	US 56545 89 A	☒	Multilayer interconnect structure for integrated circuit - has Ti/TiN stack formed over interlayer dielectric and contact openings etched in dielectric which is then filled with TiN on sides and bottom and has metal plug formed within it	
110	JP 09181 183 A	☒	Semiconductor IC device - has first wiring group which is selectively connected with second and third wiring groups in I/O and pad areas	
111	JP 09034 602 A	☒	Computer peripheral switch circuit for I/O management - performs communication through pin provided between connector of printer port and connector of printer or scanner	
112	US 55594 41 A	☒	Transmission line driver - has integrated circuit including all additional circuitry to automatically adjust matching impedance of pad drivers	
113	US 55482 80 A	☒	Hub unit for local area network - has end stations which are connected to respective groups of pins of common connector unit to communicate simultaneously and independently with hub unit	
114	JP 08184 646 A	☒	Semiconductor integrated circuit used as drive system for LCD panel - has pair of switching circuit sets which sequentially connects signal output pads and test pads by generating corresponding switching signals	
115	DE 29602 864 U	☒	Interactive TV channel transmission system using antenna network - has on-line selection connection between telephone and television set, and transmits control signals via aerial network in response to input via key-pad of telephone	
116	US 58475 78 A	☒	Programmable multiplexing input-output port - creates virtual input-output pins while using single physical pin through multiplexing techniques using input and output buffers	
117	JP 08091 078 A	☒	Automatic transmission type vehicle selection lever detent pin retention mechanism - has protrusion for detent pin provided with connection concave part set between overlapped opposite sides of leg ends	
118	EP 69680 1 A	☒	Synchronous semiconductor memory device for DRAM microprocessor - uses selected bits of internal address to access memory section and select groups of internal data lines at different frequency	

	Docum ent ID	U	Title	Current OR
119	TW 27018 9 A	<input checked="" type="checkbox"/>	Connector assembly for peripheral device - has pin arrangement configured for use by peripheral device, and determination system for communication mode of peripheral device	
120	EP 68352 8 A	<input checked="" type="checkbox"/>	Electro-optic integrated circuit including an addressable array of LEDS - having reduced size and cost due to reduced external connection pads	
121	DE 44049 22 C	<input checked="" type="checkbox"/>	Web heat treatment roller useful for avoiding heat loss at surface - comprises drillings for heat delivery and roller and flange journal drillings to prevent critical temp. differences in roller body	
122	US 54365 54 A	<input checked="" type="checkbox"/>	Computer controlled cable tester - uses computer to from test signal which via I=O port and multiplexer is applied to test point and associated connections while output state of each pin in stored recorded	
123	US 54315 83 A	<input checked="" type="checkbox"/>	Weather sealed male splice adaptor - includes tubular housing having first and second sections which are detachably coupled to one another, each including seal between output port and connector pins	
124	US 54020 14 A	<input checked="" type="checkbox"/>	Integrated circuit including peripheral port, for microprocessor - has input=output ports configured with both volatile and non-volatile configuration circuitry	
125	US 53922 97 A	<input checked="" type="checkbox"/>	Application Specific Integrated Circuit test method using configurations that can be designed into ASIC chips - generating configurations for isolation circuits so isolation circuits are transparent during normal operation of host chip but allow embedded functional blocks to be isolated and accessed for testing via host chip's pads	
126	US 53871 22 A	<input checked="" type="checkbox"/>	Pulse oximeter probe connector - with projections functioning to automatically align connector pins with sockets, connector pins being wired to sensor elements	
127	GB 22867 03 B	<input checked="" type="checkbox"/>	Programmable logic device with redundant circuitry - has normal logic groups arranged in rows and columns associated with conductors, and switches redundant logic circuitry into use in place of defective circuitry	
128	US 53296 97 A	<input checked="" type="checkbox"/>	Turning concave cut in workpiece for mfg. compliant pin connector - rotating workpiece about axis corresp. to its longitudinal axis in first direction and turning rotary cutter in second direction opposite to first	
129	EP 60297 3 A	<input checked="" type="checkbox"/>	Mixed signal integrated circuit architecture with normal and test mode operation - has mixed signal circuits separated into functional blocks on digital and analog bus with I/O multiplexers controlled by test system	
130	WO 94082 83 A	<input checked="" type="checkbox"/>	Polarity-independent connection system for electrical and electronic appliances - detects direction of insertion of component and connects one of two sets of terminal pins arranged symmetrically on connector	
131	EP 57396 5 A	<input checked="" type="checkbox"/>	Semiconductor device with multiple function selection bonding optional circuit according to power source or ground connection - has two transistors connected in parallel between bond pad and voltage terminal, of different drive capability, with larger drive transistor turned ON only for set time after device power-up, and has circuit to output pad potential signal	
132	EP 55407 7 A	<input checked="" type="checkbox"/>	Packaging system for interconnection of crosspoint switching networks - uses interconnection board between two orthogonally positioned connectors to interconnect connector pins which are not mutually aligned	
133	US 52315 89 A	<input checked="" type="checkbox"/>	Input-output pin assignment partic. for LSI device - classifying signal lines into groups depending on attributes, assigning priority level to each group w.r.t. delay time and assigning pins w.r.t. priority order	
134	ZA 92064 19 A	<input checked="" type="checkbox"/>	Electrical accessory e.g plug, adaptor for plugging electrically energisable unit into supply sockets - has switch unit connected between live pin and its connector terminal of set of pins, and operator unit for switching it between on and off	
135	US 54002 62 A	<input checked="" type="checkbox"/>	Universal interconnect matrix array - includes two sets of conductive leads formed in two directions respectively and electrical interconnecting of selected ones.	

	Docum ent ID	U	Title	Current OR
136	EP 50812 8 A	☒	Monolithic design for gallium arsenide PIN diode switch circuit - has two input and two output ports and two pairs of back-to-back monolithic PIN diodes connected between both pairs of input and output ports	
137	US 51246 38 A	☒	Automatic circuit tester employing three-dimensional switch-matrix - has scanner in main group of boards, switched by relays on auxiliary boards extending from main boards	
138	EP 49938 3 B	☒	Mixed mode analog-digital programmable interconnect IC architecture - contains user-configurable analog and digital modules, D=A and A=D converters, interconnections and I=O architecture	
139	EP 47812 1 A	☒	Multiprocessor boards signal routing system - arrays multi device processing nodes in three dimensional computing architecture and flexibly connects ports with topology of node	
140	EP 47077 0 A	☒	Test driver for connecting computer to IC chip - has data and circular shift register connected to test data input and output pin, and uses control word to test mode select pin respectively	
141	EP 45197 5 A	☒	C-, T- or S-type microwave switch for communication satellite - includes mechanical rotary-cam actuator with at least one ridge and one indentation which override pins as cam rotates	
142	EP 43812 7 A	☒	Semiconductor wafer with die-sort test pad - has connection pattern formed on dicing line area and connecting sets of pads in respective sets	
143	EP 51784 6 B	☒	Programmable logic device with programmable inverters at I=0 - including two sets of programmable lines crossing one another and connectable by programming links at each section	
144	US 50235 90 A	☒	17-Bit cascadable comparator using generic array logic - registers data applied to input pins in macro cell upon pulsing clock and any subsequent coincidence of data causes output	
145	EP 57137 3 B	☒	DC power distribution bus protection system during live serving - activates low impedance shunt after load capacitance is charged when connecting load, and is deactivated prior to disconnecting load	
146	US 49566 21 A	☒	Three-state, two-output variable RF power divider - has T-shaped and U-shaped microstrip transmission lines between input port and 2 output ports with PIN diodes connected to ground plane	
147	GB 22267 39 A	☒	Node controller for local area network - has node interface which responds to release of selected pin to activate pins w.r.t. ring bus interface	
148	DE 37812 77 G	☒	Bit resolution extension arrangement for D=A to analog converter - provides string of resistive elements connected with switches and logic gate and arranged across resistors of another string	
149	US 48127 42 A	☒	Integrated circuit package having removable test region - uses pins to test package for electrical short and open circuits, and has I=0 pins connected to signal pads	
150	DE 38230 88 A	☒	Seven pin integrated circuit component e.g. for car radio - has two amplifiers coupled for bridge or stereo operation by seventh pin comparator	
151	DE 37789 73 G	☒	Semiconductor memory device with redundancy memory cells - has pad section which receives test and address signals, memory block selector, and exchange control by-pass selective operation	
152	JP 62226 719 A	☒	Exchanging terminal for logical operation circuit - sets input pins of same logical connection for same allowable signal level, and selects matching output end line NoAbstract Dwg 1-3/8	
153	DE 36850 21 G	☒	Dual in-line package switch - has slider located by engagement of detent in recess in which it is held by cover	
154	EP 22731 2 A	☒	Retargetable buffer probe for logic analyser - accesses signals appearing at integrated circuit pins and buffers for external transmission via replacement plug assembly	

	Docum ent ID	U	Title	Current OR
155	JP 61166 258 A	<input checked="" type="checkbox"/>	Multifunction telephone set - has ten-key pad with contacts selectable for connection to either microcomputer control or telephone dialling circuit NoAbstract Dwg 3/3	
156	EP 18800 3 A	<input checked="" type="checkbox"/>	Connector pin insertion machine - has cam link mechanisms on common axis for cutting device to separate pins for pressing into board	
157	US 45677 56 A	<input checked="" type="checkbox"/>	New N-alkyl N-(3-substd.-aminophenyl 3,3,-di:methyl glutaric di:amide - useful as post=emergent herbicides	
158	EP 16384 5 A	<input checked="" type="checkbox"/>	Diagnostic protection circuit for microprocessor controller system - has circuit for diagnosing short circuit and open circuit conditions and protecting loads	
159	DE 35092 47 C	<input checked="" type="checkbox"/>	Relay multiplexer circuit for auto-test equipment pins - has test channels and pins grouped together with relays connecting any combination together within group	
160	EP 14592 5 A	<input checked="" type="checkbox"/>	Automatic path route establishment between components on substrate - using global routing on data processor to provide connections between pairs of pins using I,L,Z or U-shaped paths in rectangular grid	
161	FR 25532 46 A	<input checked="" type="checkbox"/>	Data transmission and reception module - includes microprocessor providing modulation by FSK	
162	EP 10332 2 A	<input checked="" type="checkbox"/>	Bidirectional switching circuit measuring AC data paths in LSI circuit - has logic circuit providing path with inversion between terminals and second logic circuit with multiplexers used for selecting desired path	
163	SU 10769 01 A	<input checked="" type="checkbox"/>	Number sorter with selectively alterable sorting group width - has code input unit taken across logic modules to pin board connected to logic function generators taken to AND-gates	
164	US 44327 59 A	<input checked="" type="checkbox"/>	Connector for medical liquid container - has tubular port in container with diaphragm and pin with catheter	
165	US 44202 39 A	<input checked="" type="checkbox"/>	Lens exchange mount with data transmitting electrical contacts - uses limited number of contact pins on mount surface and has switch to engage automation circuit	
166	US 43987 79 A	<input checked="" type="checkbox"/>	Keying appts. for ensuring correctness of interconnections - has fluted connector blocks to admit dowels with spacing corresponding to possible fixed locations on keying plate	
167	EP 81873 A	<input checked="" type="checkbox"/>	Microprocessor controlled data writing and reading processing system - controls logic gates and external terminal of single memory used both for writing and reading	
168	EP 81135 A	<input checked="" type="checkbox"/>	Substrate for mounting integrated circuit chips - has some solder pads for direct bonding and some with multilayer pedestal for wire bonding	
169	JP 57188 179 A	<input checked="" type="checkbox"/>	Colour switch-over appts. for adjusting TV set - has switch=over connector, connector pins surrounding switch contact points NoAbstract	
170	DE 30358 54 A	<input checked="" type="checkbox"/>	Switch box for transport container refrigeration unit - has rear connection module, intermediate HV module and front LV module to facilitate rapid repair	
171	US 41802 03 A	<input checked="" type="checkbox"/>	Programmable test point selector circuit - has digital program words from test set used to designate pins of multipin connector for use as either input or output pin	
172	BE 80578 9 A	<input checked="" type="checkbox"/>	Electrically heated glass pane - with twin element system for two level heating	

	Docum ent ID	U	Title	Current OR
102	US 49472 33 A	<input checked="" type="checkbox"/>	Semi-custom LSI having input/output cells	257/203
103	US 49301 00 A	<input checked="" type="checkbox"/>	Programmable pulse input/output processing unit having register types specified by instructions	713/502
104	US 48112 52 A	<input checked="" type="checkbox"/>	Leakage test equipment	702/51
105	US 47440 25 A	<input checked="" type="checkbox"/>	Arrangement for expanding memory capacity	711/172
106	US 46268 44 A	<input checked="" type="checkbox"/>	Addressable electronic switch	340/5.5
107	US 45190 78 A	<input checked="" type="checkbox"/>	LSI self-test method	714/728
108	US 44714 24 A	<input checked="" type="checkbox"/>	Apparatus and method for conditioning grain	700/16
109	US 44451 12 A	<input checked="" type="checkbox"/>	Positional encoders with plug-together modules	341/9
110	US 43993 54 A	<input checked="" type="checkbox"/>	Digital rate monitor	377/26
111	US 43800 70 A	<input checked="" type="checkbox"/>	Automatic circuit identifier	340/537
112	US 38724 41 A	<input type="checkbox"/>	SYSTEMS FOR TESTING ELECTRICAL DEVICES	714/25

	Document ID	U	Title	Current OR
1	US 20040 00805 1 A1	<input type="checkbox"/>	Semiconductor characteristic evaluation apparatus	324/765
2	US 20040 00157 9 A1	<input checked="" type="checkbox"/>	Systems and methods for voice and data communications including hybrid key system/PBX functionality	379/156
3	US 20040 00150 1 A1	<input checked="" type="checkbox"/>	Systems and methods for voice and data communications including a scalable TDM switch/multiplexer	370/442
4	US 20040 00147 9 A1	<input checked="" type="checkbox"/>	Systems and methods for voice and data communications including a network drop and insert interface for an external data routing resource	370/352
5	US 20030 23466 1 A1	<input checked="" type="checkbox"/>	Semiconductor device and test method for the same	324/765
6	US 20030 21902 9 A1	<input checked="" type="checkbox"/>	Systems and methods for multiple mode voice and data communications using intelligently bridged TDM and packet buses and methods for performing telephony and data functions using the same	370/442
7	US 20030 17871 6 A1	<input checked="" type="checkbox"/>	Light thin stacked package semiconductor device and process for fabrication thereof	257/686
8	US 20030 14738 1 A1	<input checked="" type="checkbox"/>	Systems and methods for multiple mode voice and data communications using intelligently bridged TDM and packet buses and methods for performing telephony and data functions using the same	370/352
9	US 20030 12085 4 A1	<input checked="" type="checkbox"/>	Method and apparatus for increasing the memory read/write speed by using internal registers	711/2
10	US 20030 03537 1 A1	<input checked="" type="checkbox"/>	Means and apparatus for a scaleable congestion free switching system with intelligent control	370/230
11	US 20030 01137 9 A1	<input checked="" type="checkbox"/>	Method for characterizing an active track and latch sense-amp (comparator) in a one time programmable (OTP) salicided poly fuse array	324/529
12	US 20020 16601 3 A1	<input checked="" type="checkbox"/>	Multi-option setting device for a peripheral control chipset	710/100
13	US 20020 08121 6 A1	<input checked="" type="checkbox"/>	CONTROL SWITCH ASSEMBLY FOR AN AIR PUMP	417/305
14	US 20020 07698 9 A1	<input checked="" type="checkbox"/>	Modular system	439/692
15	US 20020 07337 2 A1	<input checked="" type="checkbox"/>	GENERAL PORT CAPABLE OF IMPLEMENTING THE JTAG PROTOCOL	714/734
16	US 20020 05223 0 A1	<input checked="" type="checkbox"/>	Video gaming apparatus for wagering with universal computerized controller and I/O interface for unique architecture	463/10
17	US 20020 03284 3 A1	<input checked="" type="checkbox"/>	Device and method for controlling solid-state memory system	711/154

	Docum ent ID	U	Title	Current OR
18	US 20020 02914 7 A1	<input checked="" type="checkbox"/>	Alarm system using local data channel	704/500
19	US 20020 00130 2 A1	<input checked="" type="checkbox"/>	Systems and methods for multiple mode voice and data communications using intelligently bridged TDM and packet buses and methods for performing telephony and data functions using the same	370/352
20	US 20020 00130 1 A1	<input checked="" type="checkbox"/>	SYSTEMS AND METHODS FOR MULTIPLE MODE VOICE AND DATA COMMUNICATIONS USING INTELLIGENTLY BRIDGED TDM AND PACKET BUSES AND METHODS FOR PERFORMING TELEPHONY AND DATA FUNCTIONS USING THE SAME	370/352
21	US 20010 05530 8 A1	<input checked="" type="checkbox"/>	SYSTEMS AND METHODS FOR MULTIPLE MODE VOICE AND DATA COMMUNICATIONS USING INTELLIGENTLY BRIDGED TDM AND PACKET BUSES AND METHODS FOR PERFORMING TELEPHONY AND DATA FUNCTIONS USING THE SAME	370/401
22	US 20010 05371 2 A1	<input checked="" type="checkbox"/>	VIDEO GAMING APPARATUS FOR WAGERING WITH UNIVERSAL COMPUTERIZED CONTROLLER AND I/O INTERFACE FOR UNIQUE ARCHITECTURE	463/1
23	US 20010 05091 8 A1	<input checked="" type="checkbox"/>	SYSTEMS AND METHODS FOR MULTIPLE MODE VOICE AND DATA COMMUNICATIONS USING INTELLIGENTLY BRIDGED TDM AND PACKET BUSES AND METHODS FOR PERFORMING TELEPHONY AND DATA FUNCTIONS USING THE SAME	370/442
24	US 66676 34 B2	<input checked="" type="checkbox"/>	Multi-option setting device for a peripheral control chipset	326/38
25	US 66666 89 B1	<input checked="" type="checkbox"/>	Electrical connector with interspersed entry ports for pins of different LEDs	439/56
26	US 65602 22 B1	<input checked="" type="checkbox"/>	Systems and methods for multiple voice and data communications using intelligently bridged TDM and packet buses and methods for performing telephony and data functions using the same	370/353
27	US 65429 96 B1	<input checked="" type="checkbox"/>	Method of implementing energy-saving suspend-to-RAM mode	713/300
28	US 65295 02 B2	<input checked="" type="checkbox"/>	Systems and methods for multiple mode voice and data communications using intelligently bridged TDM and packet buses and methods for performing telephony and data functions using the same	370/353
29	US 64987 91 B2	<input checked="" type="checkbox"/>	Systems and methods for multiple mode voice and data communications using intelligently bridged TDM and packet buses and methods for performing telephony and data functions using the same	370/353
30	US 64684 39 B1	<input checked="" type="checkbox"/>	Etching of metallic composite articles	216/95
31	US 64456 82 B1	<input checked="" type="checkbox"/>	Systems and methods for multiple mode voice and data communications using intelligently bridged TDM and packet buses and methods for performing telephony and data functions using the same	370/257
32	US 64307 19 B1	<input checked="" type="checkbox"/>	General port capable of implementing the JTAG protocol	714/734
33	US 64154 07 B1	<input checked="" type="checkbox"/>	Debugging device for a system controller chip to correctly lead its signals to IC leads	714/734
34	US 64111 23 B1	<input checked="" type="checkbox"/>	Multi-option setting device for peripheral control chipset	326/38
35	US 64099 30 B1	<input checked="" type="checkbox"/>	Lamination of circuit sub-elements while assuring registration	216/13
36	US 64007 11 B1	<input checked="" type="checkbox"/>	Systems and methods for multiple mode voice and data communications using intelligently bridged TDM and packet buses and methods for performing telephony and data functions using the same	370/353

	Docum ent ID	U	Title	Current OR
37	US 63985 08 B1	<input checked="" type="checkbox"/>	Control switch assembly for an air pump	417/33
38	US 63968 49 B1	<input checked="" type="checkbox"/>	Systems and methods for multiple mode voice and data communications using intelligently bridged TDM and packet buses and methods for performing telephony and data functions using the same	370/490
39	US 63851 94 B2	<input checked="" type="checkbox"/>	Systems and methods for multiple mode voice and data communications using intelligently bridged TDM and packet buses and methods for performing telephony and data functions using the same	370/353
40	US 63665 78 B1	<input checked="" type="checkbox"/>	Systems and methods for multiple mode voice and data communications using intelligently bridged TDM and packet buses and methods for implementing language capabilities using the same	370/353
41	US 63650 57 B1	<input checked="" type="checkbox"/>	Circuit manufacturing using etched tri-metal media	216/13
42	US 63626 49 B1	<input checked="" type="checkbox"/>	Field programmable gate array with mask programmed input and output buffers	326/41
43	US 63565 54 B1	<input checked="" type="checkbox"/>	Systems and methods for multiple mode voice and data communications using intelligently bridged TDM and packet buses and methods for performing telephony and data functions using the same	370/402
44	US 63113 03 B1	<input checked="" type="checkbox"/>	Monitor port with selectable trace support	714/734
45	US 62980 45 B1	<input checked="" type="checkbox"/>	Systems and methods for multiple mode voice and data communications using intelligently bridged TDM and packet buses and methods for performing telephony and data functions using the same	370/261
46	US 62890 25 B1	<input checked="" type="checkbox"/>	Systems and methods for multiple mode voice and data communications using intelligently bridged TDM and packet buses and methods for performing telephony and data functions using the same	370/458
47	US 62663 41 B1	<input checked="" type="checkbox"/>	Systems and methods for multiple mode voice and data communications using intelligently bridged TDM and packet buses and methods for performing telephony and data functions using the same	370/458
48	US 62663 40 B1	<input checked="" type="checkbox"/>	Systems and methods for multiple voice data communication which includes interface cards including configurable clocks that are dynamically coupled to a TDS bus	370/442
49	US 62625 94 B1	<input checked="" type="checkbox"/>	Apparatus and method for configurable use of groups of pads of a system on chip	326/38
50	US 62302 76 B1	<input checked="" type="checkbox"/>	Energy conserving measurement system under software control and method for battery powered products	713/320
51	US 61544 65 A	<input checked="" type="checkbox"/>	Systems and methods for multiple mode voice and data communications using intelligently bridged TDM and packet buses and methods for performing telephony and data functions using the same	370/466
52	US 61483 98 A	<input checked="" type="checkbox"/>	Setting/driving circuit for use with an integrated circuit logic unit having multi-function pins	713/1
53	US 61483 63 A	<input checked="" type="checkbox"/>	Device and method for controlling solid-state memory system	711/103
54	US 61474 19 A	<input checked="" type="checkbox"/>	Output-motor assembly	307/116
55	US 61007 43 A	<input checked="" type="checkbox"/>	Circuit arrangement for adding functionality to a circuit with reduced propagation delays	327/374
56	US 60972 18 A	<input checked="" type="checkbox"/>	Method and device for isolating noise sensitive circuitry from switching current noise on semiconductor substrate	326/82

	Document ID	U	Title	Current OR
57	US 5991232 A	<input checked="" type="checkbox"/>	Clock synchronous memory embedded semiconductor integrated circuit device	365/233
58	US 5963746 A	<input checked="" type="checkbox"/>	Fully distributed processing memory element	712/20
59	US 5962868 A	<input checked="" type="checkbox"/>	Semiconductor device having contact check circuit	257/48
60	US 5959466 A	<input checked="" type="checkbox"/>	Field programmable gate array with mask programmed input and output buffers	326/39
61	US 5949984 A	<input checked="" type="checkbox"/>	Emulator system	703/23
62	US 5917362 A	<input checked="" type="checkbox"/>	Switching circuit	327/408
63	US 5859523 A	<input checked="" type="checkbox"/>	Rechargeable battery pack for battery powered devices with a rotatably mounted plug	320/111
64	US 5822610 A	<input checked="" type="checkbox"/>	Mappable functions from single chip/multi-chip processors for computers	712/39
65	US 5821776 A	<input checked="" type="checkbox"/>	Field programmable gate array with mask programmed analog function circuits	326/41
66	US 5819025 A	<input checked="" type="checkbox"/>	Method of testing interconnections between integrated circuits in a circuit	714/30
67	US 5796965 A	<input checked="" type="checkbox"/>	Intelligent power circuit for external data drive	713/340
68	US 5739666 A	<input checked="" type="checkbox"/>	Rechargeable battery pack for battery powered devices	320/113
69	US 5739455 A	<input checked="" type="checkbox"/>	Electronic guitar music simulation system	84/615
70	US 5735155 A	<input checked="" type="checkbox"/>	Method for manufacturing patterned tread plates	72/14.8
71	US 5731526 A	<input checked="" type="checkbox"/>	System for displaying the amount of fluid dispensed from a hand-held sprayer	73/861
72	US 5717943 A	<input checked="" type="checkbox"/>	Advanced parallel array processor (APAP)	712/20
73	US 5689172 A	<input checked="" type="checkbox"/>	Charging battery system for video camera	320/125
74	US 5670955 A	<input checked="" type="checkbox"/>	Method and apparatus for generating directional and force vector in an input device	341/34
75	US 5655142 A	<input checked="" type="checkbox"/>	High performance derived local bus and computer system employing the same	712/32
76	US 5630170 A	<input checked="" type="checkbox"/>	System and method for determining peripheral's communication mode over row of pins disposed in a socket connector	710/12
77	US 5608686 A	<input checked="" type="checkbox"/>	Synchronous semiconductor memory device with low power consumption	365/233
78	US 5565766 A	<input checked="" type="checkbox"/>	Semiconductor circuit element device with arrangement for testing the device and method of test	324/158.1
79	US 5555420 A	<input checked="" type="checkbox"/>	Multiprocessor programmable interrupt controller system with separate interrupt bus and bus retry management	710/266

	Docum ent ID	U	Title	Current OR
80	US 55401 02 A	<input checked="" type="checkbox"/>	System for displaying the amount of fluid dispensed from a hand-held sprayer	73/861
81	US 55262 78 A	<input checked="" type="checkbox"/>	Method and apparatus for converting field-programmable gate array implementations into mask-programmable logic cell implementations	716/16
82	US 54956 15 A	<input checked="" type="checkbox"/>	Multiprocessor interrupt controller with remote reading of interrupt control registers	710/260
83	US 54597 37 A	<input checked="" type="checkbox"/>	Test access port controlled built in current monitor for IC devices	714/733
84	US 54554 68 A	<input checked="" type="checkbox"/>	Switching circuit for switching a plurality of lines	307/112
85	US 54324 41 A	<input checked="" type="checkbox"/>	Testability architecture and techniques for programmable interconnect architecture	324/158 .1
86	US 54308 59 A	<input checked="" type="checkbox"/>	Solid state memory system including plural memory chips and a serialized bus	711/103
87	US 54288 06 A	<input checked="" type="checkbox"/>	Computer networking system including central chassis with processor and input/output modules, remote transceivers, and communication links between the transceivers and input/output modules	710/104
88	US 54188 91 A	<input checked="" type="checkbox"/>	Printer sharing device	358/1.1 5
89	US 54107 10 A	<input checked="" type="checkbox"/>	Multiprocessor programmable interrupt controller system adapted to functional redundancy checking processor systems	710/266
90	US 54020 14 A	<input checked="" type="checkbox"/>	Peripheral port with volatile and non-volatile configuration	326/37
91	US 53069 57 A	<input checked="" type="checkbox"/>	Switch lever operating device with automatic timer	307/141
92	US 53032 46 A	<input checked="" type="checkbox"/>	Fault isolation diagnostics	714/727
93	US 53008 11 A	<input checked="" type="checkbox"/>	Integrated circuit device and microprocessor constituted thereby	257/691
94	US 52166 23 A	<input checked="" type="checkbox"/>	System and method for monitoring and analyzing energy characteristics	702/62
95	US 51344 69 A	<input checked="" type="checkbox"/>	Endoscope light source apparatus with detachable flash unit	348/68
96	US 51014 98 A	<input checked="" type="checkbox"/>	Pin selectable multi-mode processor	710/316
97	US 50972 13 A	<input checked="" type="checkbox"/>	Apparatus for automatic testing of electrical and electronic connectors	324/538
98	US 50381 19 A	<input checked="" type="checkbox"/>	Piezoelectric oscillator semiconductor circuit with oscillation circuit adjustment means	331/158
99	US 50288 21 A	<input checked="" type="checkbox"/>	Programmable logic device with programmable inverters at input/output pads	326/41
100	US 49856 41 A	<input checked="" type="checkbox"/>	Semiconductor integrated circuit device having selectable operational functions	327/198
101	US 49473 57 A	<input checked="" type="checkbox"/>	Scan testing a digital system using scan chains in integrated circuits	714/726